

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Cancelled)

2. (New) A method of programming a PMOS stacked-gate memory cell, wherein the memory cell includes a p-type source region formed in n-type semiconductor material, a p-type drain region formed in the n-type semiconductor material and spaced-apart from the p-type source region to define a substrate channel region therebetween, a conductive floating gate electrode formed over the substrate channel region and separated therefrom by gate dielectric material, and a conductive control gate electrode formed over the floating gate electrode and separated therefrom by intergrate dielectric material, the programming method comprising:

- (a) applying a negative voltage potential to the p-type drain region;
- (b) applying a voltage pulse to the control gate electrode such that electrons are attached to the floating gate electrode from the p-type drain region through the gate dielectric material;
- (c) repeating step (b) above to provide a sequence of voltage pulses to the control gate electrode such that sufficient electrons are attached to the floating gate electrode to bring the floating gate electrode from an initial voltage potential to a selected voltage potential that is negative and lower in absolute value than the negative voltage potential applied to the p-type drain region.

3. (New) A programming method as in claim 2, and wherein a coupling coefficient exists between the floating gate electrode and the control gate electrode, and wherein the step up in each pulse in the sequence of voltage pulses provided to the control gate is approximately equal

to the difference between the initial voltage potential and the selected voltage potential of the floating gate electrode divided by the coupling coefficient.

4. (New) A programming method as in claim 3, and wherein the time between the voltage pulses applied to the control gate electrode is sufficient to allow the floating gate electrode to come to the selected voltage potential.
5. (New) The programming method of claim 2, and wherein the semiconductor material is n-type silicon.
6. (New) The programming method of claim 5, and wherein the gate dielectric material is silicon dioxide.
7. (New) The programming method of claim 6, and wherein the floating gate electrode is polysilicon.
8. (New) The programming method of claim 7, and wherein the control gate electrode is polysilicon.